Remarks:

The preliminary amendment is being filed in an effort to present an application in proper U.S. format and to present claims in proper U.S. claim idiom for examination.

The newly entered claims are fully supported in the originally presented claims and in the claims of the German priority application.

An early action on the merits of the claims is requested.

Respectfully submitted,

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Jenoe Tihanyi

Applic. No. : 10/007,397

Filed

: October 22, 2001

Title : Semiconductor Component

PRELIMINARY AMENDMENT

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Translated Specification:

On page 1, line 1 through page 2, line 14:

[Description

Semiconductor component] SEMICONDUCTOR COMPONENT

Background of the Invention:

Field of the Invention:

The present invention relates to a semiconductor component, in particular a field-effect-controllable transistor.

DE 198 28 191 C1 discloses a lateral high-voltage transistor having, on an n-conducting substrate, an epitaxial layer in which source and drain zones and also a channel zone

in the epitaxial layer. [, the sidewalls of which] The sidewalls of these trenches are heavily doped with a complementary dopant with respect to the rest of the epitaxial layer. A conductive channel in the channel zone can be controlled by means of a gate electrode insulated from the channel zone.

When a source-drain voltage is applied, a space charge zone propagates in this transistor - if no gate-source voltage is applied - proceeding from the source zone, and[,] as the voltage rises, the space charge zone gradually reaches the complementarily doped sidewalls of the trenches in the direction of the drain zone. Where the space charge zone propagates, free charge carriers of the doped sidewalls of the trenches and free charge carriers of the surrounding epitaxial layer mutually compensate one another. In these regions in which the free charge carriers mutually compensate one another, a high breakdown voltage results for lack of free charge carriers. The reverse voltage of the transistor can be set by means of the doping of the trenches, the epitaxial layer preferably being highly doped, as a result of which the transistor has a low on resistance when the gate is driven.

Such transistors having a low on resistance but a high reverse voltage are currently available only as discrete components,

that is to say of the transistor is realized in a semiconductor body. However, for many applications, for example for switching loads, it is desirable to integrate a transistor as a switching element and its associated drive circuit, for example using CMOS technology, in a single semiconductor body.

[This goal is achieved by means of a semiconductor component in accordance with the features of claim 1.

The subclaims relate to advantageous refinements of the invention.]

Summary of the Invention:

On page 5, line 27 through page 6, line 28:

[The present invention is explained in more detail below using exemplary embodiments with reference to figures, in which:

figure 1 shows a first exemplary embodiment of a semiconductor component according to the invention in a lateral sectional illustration;

figure 2 shows a semiconductor component according to the invention according to an embodiment with elongate first terminal zones in a sectional illustration in plan view;

figure 3 shows a semiconductor component according to the invention with an annularly closed first terminal zone in a lateral sectional illustration in plan view;

figure 4 shows a semiconductor component according to the invention according to a further embodiment of the invention in a lateral sectional illustration;

figure 5 shows a semiconductor component with a plurality of first terminal zones and compensation zones running in a pillar-shaped manner in a lateral sectional illustration;

figure 6 shows a semiconductor component with a plurality of first terminal zones and compensation zones of spherical design in a lateral sectional illustration;

figure 7 shows a semiconductor component with a plurality of first terminal zones and first and second compensation zones arranged adjacent in a lateral sectional illustration; and

figure 8 shows a semiconductor component according to the invention with a plurality of first terminal zones and a second terminal zone surrounding the first terminal zones in a well-like manner, in a lateral sectional illustration.]

Fig. 1 is a cross sectional view of a first exemplary embodiment of a semiconductor component;

Fig. 2 is a plan view of an embodiment of a semiconductor component with elongate first terminal zones;

Fig. 3 is a plan view of an embodiment of a semiconductor component with an annularly closed first terminal zone;

Fig. 4 is a cross sectional view of another exemplary embodiment of a semiconductor component;

Fig. 5 is a cross sectional view of another exemplary
embodiment of a semiconductor component with a plurality of
first terminal zones and compensation zones running in a
pillar-shaped manner;

Fig. 6 is a cross sectional view of another exemplary

embodiment of a semiconductor component with a plurality of

first terminal zones and compensation zones of spherical

design;

Fig. 7 is a cross sectional view of another exemplary embodiment of a semiconductor component with a plurality of

first terminal zones and with first compensation zones adjacent second compensation zones; and

Fig. 8 is a cross sectional view of another exemplary

embodiment of a semiconductor component with a plurality of

first terminal zones and with a second terminal zone

surrounding the first terminal zones in a well-like manner.

Description of the Preferred Embodiments:

On page 8, lines 23-30:

[p-doped] <u>P-doped</u> compensation zones 30 are formed in the n-doped layer 24, and[,] in the exemplary embodiment [according to] <u>shown in figure 1</u>, <u>the compensation zones</u> extend in a pillar-shaped manner in the vertical direction of the semiconductor body 20. The cross section of these pillars 30 is circular in the exemplary embodiments [according to] <u>shown in figures 2</u> and 3, but this cross section can assume virtually any other geometric [shapes] <u>shape</u> and <u>can</u> be, for example, rectangular, square or octagonal.

On page 18:

[List of reference symbols

Semiconductor body

20

22	Substrate
24	First n-conducting layer
26	Second n-conducting layer
30, 30A	Compensation zone
32	p-conducting layer
40	Source zone
50, 50A, 50B, 50C	Channel zone
52	Source electrode
60	Drain zone
62	Drain electrode
70	Gate electrode
70A, 70B, 70C, 70D	Gate electrodes
72	Insulation layer
72A, 72B, 72C, 72D	Insulation layers
80	Boundary zone
90	Boundary zone Metalization layer
	Metalization layer
90	Metalization layer
90 90, 91, 92, 93, 94	Metalization layer Field plates
90 90, 91, 92, 93, 94 95	Metalization layer Field plates Field plate
90 90, 91, 92, 93, 94 95 124	Metalization layer Field plates Field plate n-conducting layer
90 90, 91, 92, 93, 94 95 124 126	Metalization layer Field plates Field plate n-conducting layer n-conducting layer
90 90, 91, 92, 93, 94 95 124 126 201	Metalization layer Field plates Field plate n-conducting layer n-conducting layer
90 90, 91, 92, 93, 94 95 124 126 201 body	Metalization layer Field plates Field plate n-conducting layer n-conducting layer First surface of the semiconductor
90 90, 91, 92, 93, 94 95 124 126 201 body T1, T2	Metalization layer Field plates Field plate n-conducting layer n-conducting layer First surface of the semiconductor CMOS transistors

 $+U_{D}$

Drain potential

n

n-doped zone

р

p-doped zone]

On page 19, line 1, [Patent Claims] I claim:

After page 21:

-- ABSTRACT OF THE DISCLOSURE:

A semiconductor component includes a semiconductor body having a substrate of a first conduction type and a first layer of a second conduction type that is located above the substrate. A channel zone of the first conduction type is formed in the first layer. A first terminal zone of the second conduction type is configured adjacent the channel zone. A second terminal zone of the first conduction type is formed in the first layer. Compensation zones of the first conduction type are formed in the first layer. A second layer of the second conduction type is configured between the substrate and the compensation zones.